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[METHOD AND SYSTEM FOR EVALUATING TIMING IN AN INTEGRATED CIRCUIT]

Abstract

Methods for analyzing the timing in integrated circuits and for reducing the pessimism in timing slack calculations in static timing analysis (STA). The methods involve grouping and canceling the delay contributions of elements having similar delays in early and late circuit paths. An adjusted timing slack is calculated using the delay contributions of elements having dissimilar delays. In some embodiments, the delay contributions of elements having dissimilar delays are root sum squared. Embodiments of the invention provide methods for reducing the pessimism due to both cell-based and wire-dependent delays. The delays considered in embodiments of the invention may include delays due to the location of elements in a path.